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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,594	03/23/2001	Yasuhiro Yoshida	55707(904)	7185
21874	7590	01/10/2005	EXAMINER	
EDWARDS & ANGELL, LLP			GOOD JOHNSON, MOTILEWA	
P.O. BOX 55874			ART UNIT	
BOSTON, MA 02205			PAPER NUMBER	
			2672	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/815,594

Applicant(s)

YOSHIDA ET AL.

Examiner

Motilewa A. Good-Johnson

Art Unit

2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-55 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10-18, 20-22, 26-34, 38-46, 48-50 and 52-54 is/are rejected.
- 7) ☒ Claim(s) 9, 19, 23-25, 35-37, 47, 51 and 55 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>09/16/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is responsive to the following communications: Application, filed 03/23/2001; IDS, paper #2, filed 06/07/2001; IDS, paper #4, filed 04/15/2003; IDS, paper #8; IDS, paper #9, Amendment A, filed 11/24/2003; Amendment B, filed 08/17/2004; IDS, filed 09/17/2004.

This action is non-final.

2. Claims 1-55 are pending in this application.
3. The present title of this application is "Image Processing Apparatus and Image Display Apparatus Using Same" (as originally filed)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-8, 10-18, 20-22, 26-34, 38-46, 48-50 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clatanoff et al., U.S. Patent Number 6,052,491, "Non-Monotonic Contour Diffusion and Algorithm", class 382/275, 04/18/2000, in view of Funke et al., U.S. Patent Number 6,724,437, "Method and Device for Adding Noise to a Video Signal for Improving a Display of the Video Signal", class 348/622, 04/20/2004, filed 12/22/1998.

Regarding claim 1, Clatanoff discloses a first signal processing circuit (figure 14, element 308) for applying gamma correction to an n-bit digital signal inputted as a video signal (col. 6, lines 4-5), and for converting the digital signal into an m-bit digital signal (col. 6, lines 5-6); and a second signal processing circuit (figure 14, element 1404); outputting a truncated integer portion of the resulting output m-bit digital signal (col. 6, lines 4-17)

However it is noted that Clatanoff fails to disclose for adding a noise signal to the m-bit digital signal.

Funke discloses adding a noise signal (col. 1, lines 55-57) to the m-bit digital signal (i.e. output signal) from said first signal processing circuit of a gamma correction circuit.

It would have been obvious to one ordinary skill in the art at the time of the invention to include adding a noise signal in the error signal processing circuit of the output signal as disclosed in Clatanoff, as disclosed in Funke, because noise removes the non-moving dither patterns of the converted signal and further improves the gray-scale reproduction for true colors.

Regarding claim 2, Clatanoff discloses first signal processing circuit includes bit-converting means for converting the inputted n-bit digital signal into the m-bit digital signal in accordance with a pre-set value (col. 5, lines 20-30)

Regarding claim 3, Clatanoff discloses bit-converting means is a look up table, which outputs the m-bit digital signal that is the present value in accordance with the inputted n-bit digital signal (col. 6, lines 35-43)

Regarding claim 4, Clatanoff discloses said bit converting means is a calculating device for converting the n-bit digital signal into the m-bit . . . digital signal by numerical calculation (col. 6, lines 55-67)

Regarding claim 5, Clatanoff discloses said first signal processing circuit and said second signal processing circuit are provided for respective RGB colors (col. 4, lines 38-42)

Regarding claim 6, Clatanoff discloses an average value of a signal level is set to zero (col. 7, lines 11-38)

Regarding claim 7, Funke discloses the noise signal is a random noise signal with no regularity in its cycle of amplitude (col. 1, line 64)

Regarding claim 8, Funke discloses the noise signal is obtained from, by using an arbitrary noise pattern table, switching a starting point of the noise pattern table per field or per noise pattern table (col. 57-61, furthermore Clatanoff discloses a bit pattern for the signal obtained, col. 7, lines 19-34)

Regarding claim 10, Clatanoff discloses an image processing apparatus, comprising: a signal processing circuit (figure 14, element 308) and for outputting a Q-bit digital signal obtained from rounding off a less significant bit from the m-bit digital signal. (col. 6, lines 4-17)

However it is noted that Clatanoff fails to disclose for adding a noise signal to an inputted m-bit digital signal.

Funke discloses adding a noise signal (col. 1, lines 55-57) to the m-bit digital signal (i.e. output signal) from said first signal processing circuit of a gamma correction circuit.

It would have been obvious to one ordinary skill in the art at the time of the invention to include adding a noise signal in the error signal processing circuit of the output signal as disclosed in Clatanoff, as disclosed in Funke, because noise removes the non-moving dither patterns of the converted signal and further improves the gray-scale reproduction for true colors.

Regarding claim 11, Clatanoff discloses display means (figures 13 and 14, element 314) for displaying an image; and driving means for driving the display means. (col. 4, lines 7-42)

Regarding claim 12, it is rejected based upon similar rational as above dependent claim 2.

Regarding claim 13, Clatanoff discloses the pre-set value in said bit converting means is rewritable so that unevenness in properties of said driving means may be absorbed (col. 8, lines 1-5)

Regarding claim 14, Clatanoff discloses the pre-set value in said bit converting means is rewritten in accordance with brightness in surrounding of said image display apparatus (col. 8, lines 1-19)

Regarding claim 15, Clatanoff discloses the pre-set value in said bit converting means is rewritten in accordance with brightness of overall display image of said display means (col. 8, lines 1-19)

Regarding claim 16, it is rejected based upon similar rational as claim 10.

Regarding claim 17, it is rejected based similar rational as claim 1.

Regarding claim 18, Funke discloses second signal processing circuit includes:
a noise generating circuit . . . (figure 1); an adding circuit for adding the noise signal . . .
(figure 1) further see above rational for claim 1.

Regarding claim 20, it is rejected based upon similar rational as claim 11.

Regarding claim 21, Clatanoff discloses the display means is a liquid crystal
display (col. 4, lines 40-42)

Regarding claim 22, Clatanoff discloses the image processing apparatus is
separately provided. (figures 13 and 14)

Regarding claim 26, Clatanoff discloses the display means is a liquid crystal
display (col. 4, lines 40-42)

Regarding claims 27-34, they are rejected based upon similar rational as above
claims 1-8 respectively.

Regarding claims 38-42, see above rejection for claims 11-15 respectively.

Regarding claims 43-46, they are rejected based upon similar rational as above
claims 1, 2, 6 and 7.

Regarding claims 48-50 and 52-54, they are rejected based upon similar rational
as above claims 6-8 respectively.

Allowable Subject Matter

6. Claims 9, 19, 23-25, 35-37, 41, 51 and 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

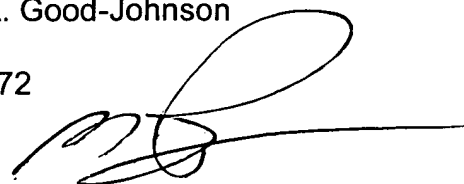
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Motilewa A. Good-Johnson whose telephone number is (703) 305-3939. The examiner can normally be reached on Monday - Friday 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (703) 305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mgj

Motilewa A. Good-Johnson
Examiner
Art Unit 2672



MICHAEL RAZAVI
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